REMARKS

This submission accompanies a Request for Continued Examination.

Claims 1-25 are pending in the above-referenced patent application. The Examiner indicated in the advisory action dated April 13, 2005 that claims 6, 7, 9, 10, 12-14 and 21 were allowable.

Applicant has amended independent claim 1 to clarify that the various contexts being swapped correspond to different threads. Support for this clarifying amendment is found throughout the application including, for example, at page 28, lines 11-20, page 29, line 22 to page 30, line 12, and so forth. Independent claims 15, 22, and 24 were similarly amended. Additionally, applicant has removed the wording "out to memory," previously appearing in claims 1 and 16, for greater clarity, and has corrected a typographical error in claim 1. Applicant has amended claims 15, 22, and 24 to clarify that swapping is performed in accordance with the evaluated specified parameter.

Additionally, applicant has amended claim 2 to recite the feature, appearing in claim 23, that waking up a swapped out context is performed using a signal specified in a context-swap program instruction. Applicant has similarly amended claim 25.

The Examiner rejected claims 1, 15, 16, 20, 22, and 24 under 35 U.S.C. §102(a) and (b) as being anticipated by U.S. Patent No. 4,868,735 to Moller. The Examiner also rejected claims 2, 3, 8, 17, 23, and 25 under 35 U.S.C. §103(a) over Moller in view of U.S. Patent No. 5,247,671 to Adkins, claims 4, 18 under 35 U.S.C. §103(a) over Moller in view of Adkins and further in view of U.S. Patent No. 5,541,920 to Angle, claims 5 and 19 under 35 U.S.C. §103(a) over Moller in view of Adkins and further in view of U.S. Patent No. 5,610,864 to Manning, and claim 11 under 35 U.S.C. §103(a) over Moller in view of Adkins and further in view of U.S. Patent No. 6,505,229 to Turner.

Applicant's independent claim 1 discloses a method that includes directing the processor to swap a currently running context, corresponding to a first thread, in a specified microengine with a different context corresponding to a different thread. By contrast, Moller describes a microprogram sequence controller that includes instruction decode circuitry to allow the controller to process microinstructions (col. 2, lines 63-66). Among other things, Moller

describes a LIFO stack 136 that facilitates interrupt handling functions (see, for example, col. 14, lines 13-37). Moller also describes a SWAP microinstruction which causes a CMUXCTL signal to be generated to cause multiplexer C-MUX 118 to pass the top of the LIFO stack 136 to a down counter (col. 30, lines 39-44). However, nowhere does Moller disclose or suggest swapping of contexts corresponding to different threads. Indeed, Moller does not at all discuss or contemplate multithread execution. So Moller does not disclose "directing the processor having a plurality of microengines to swap a currently running context, corresponding to a first thread, in a specified microengine out to memory to let another context, corresponding to a different thread, execute in that microengine and cause a different context and associated program counter to be selected," as required by applicant's independent claim 1.

Rejected claims 2-5, 8, and 11 depend from independent claim 1 and are thus patentable for at least the same reasons as independent claim 1.

Claims 15, 22, and 24 respectively claim a method, processor, and computer program product featuring "evaluating a parameter to determine a state of an executing context process corresponding to a first thread; and performing a swapping operation to cause a different context and associated program counter, corresponding to a different thread, to be selected in accordance with the value of the evaluated specified parameter," or similar language. For similar reasons as those provided with respect to independent claim 1, at least this feature is not disclosed by the art.

Rejected claims 16-20, which depend from independent claim 15, are patentable for at least the same reasons as claim 15. Rejected claim 23, which depends from independent claim 22, is patentable for at least the same reasons as claim 22. Rejected claim 25, which depends from independent claim 24, is patentable for at least the same reasons as claim 24.

In addition, as noted above, the Examiner has rejected claims 2, 23, and 25 under 35 U.S.C. §103 (a) over Moller in view of Adkins.

Applicant's claim 2 recites that the processor wakes up the swapped out context when a signal specified in a context-swap program instruction is activated. Thus, the swapping operation is performed in accordance with a signal identified in a program instruction.

As previously explained, Moller discloses a SWAP microinstruction (Moller's col. 30, line 40). However, Moller explains that, "[e]ach "machine" instruction is implemented on the

microprocessor by a sequence of microinstructions selected by the microprogram sequence controller 10" (emphasis added, col. 4, lines 50-53). In other words, a microinstruction is but a single step in the execution of one (1) program instruction, and it configures the microprocessor in a particular way (e.g., activating a bus or some control signal). Moller's microinstructions, including the SWAP microinstruction do not suggest the features of the context-swap program instruction recited in applicant's claim 2. Moreover, none of Moller's microinstructions wakes up the swapped out context when a specified signal specified in the context-swap instruction is activated, as also required by applicant's claim 2.

Adkins describes a scheduler executing on a serial communications adapter that schedules tasks at different priority levels (Abstract). While Adkins describes that a sleeping task can be awakened and have its context restored when a new event associated with that task arrives at the port response queue (col. 8, lines 36-57), nowhere does Adkins describe that waking up a context is achieved when a signal, specified in a program instruction, is activated. Indeed, Adkins does not disclose or suggest use of program instructions to control swapping as does applicant's claim 2.

Since neither Moller nor Adkins discloses or suggests, alone or in combination, the feature of "directing the processor wakes up the swapped out context when a signal specified in a context-swap program instruction is activated," applicant's claim 2 is patentable over the cited art.

Rejected claims 3-5, 8, and 11, which depend from claim 2, are patentable for at least the same reasons as claim 2.

Claims 23 and 25 respectively recite a processor and computer program product, each featuring "the context swap instruction wakes up the swapped out context when a specified signal is activated," or similar language. For similar reasons as those provided with respect to claim 2, at least this feature is not disclosed by the art.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made

arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Applicants enclose a Petition for One Month Extension of Time, with the required fee of $120. Please apply any other charges to deposit account 06-1050, referencing attorney docket 10559-303US1.

Respectfully submitted,

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